Datasheet ADQ8-8C

ADQ8-8C is a digitizer for modular instrumentation.
ADQ8-8C is intended for large scale integration and features:

- *8 analog channels*
- *10 bits vertical resolution*
- *1 GSPS per channel*
- *Multi-unit synchronization for large installations*
- *Open FPGA for custom real-time applications (option)*


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Teledyne Signal Processing Devices Sweden AB | Teknikringen 6, SE-583 30 Linköping, Sweden | www.spdevices.com
Regional sales offices | www.spdevices.com/contact

ADQ8-8C Datasheet

Features

- 8 analog channels
- 1 GSPS sample rate per channel
- 10 bits vertical resolution
- Input impedance 50 Ω and 1 MΩ
- DC-coupled
- 500 MHz analog bandwidth
- Digital filter for bandwidth control
- Programmable DC-offset
- High sensitivity input
- Vertical range setting
- Over-voltage protection
- Internal clock reference
- Backplane clock reference
- One channel dedicated for external trigger with trigger time interpolation
- External trigger
- Multi-unit synchronization
- Time-stamp for real-time operation
- 1 GBytes data memory
- 2.6 GBytes/s data streaming
- Data interface PXIe and MTCA.4

Applications

- Ultrasound applications
- Non-destructive testing
- Wireless communication
- Time-of-flight
- Scientific instruments
- Particle physics
- Semiconductor test
- ATE
- Test and measurement
- Quantum technology

Advantages

- Host PC interface options and large scale integration support for optimized system's partitioning.
- Advanced analog front-end and high sample rate for meeting detector and measurement requirements.
- Application specific firmware options and real-time custom processing solutions for advanced systems for optimized cost of ownership.
- SP Devices' design services are available for fast integration to lower time-to-market.

Options summary

ORDER CODE	NAME	DESCRIPTION
–VG[1]	Full flexible analog front-end	Flexible analog front-end including user controlled DC-offset, impedance and voltage range.
–PXIE	PXI Express format	Form factor for integration in a PXI Express 3U chassis
–MTCA	MTCA.4 format	Form factor for integration in a MTCA.4 chassis.
–FWDAQ[2]	Data acquisition firmware	Data acquisition functions.
–DEV8DAQ[3]	Firmware development kit	Open the FPGA to add custom firmware to –FWDAQ.
–W5Y	Warranty 5 years	Warranty extended from 3 to 5 years[4 5]

1. Always included with the ADQ8-8C.
2. Always included with the ADQ8-8C.
3. Purchased separately.
4. Included warranty is 3 years from the date the product is shipped by Teledyne SP Devices. This option extends the warranty to 5 years from the date the product is shipped by Teledyne SP Devices.
5. Warranty extension must be ordered before included 3 years warranty is expired.

1 Technical data

All values are typical unless otherwise noted.

Table 1: Analog input –VG

PARAMETER		–PXIE	–MTCA
Analog inputs 50 Ω and 1 MΩ modes [1] [2]			
Connector		LEMO00	SMA
Coupling		DC	DC
Input range settings	[V_{pp}]	0.25 0.5 1 2.5 5	0.25 0.5 1 2.5 5
Variable DC-offset	[V]	± 0.5 * range [3]	± 0.5 * range [4]
Cross talk isolation DC – 500 MHz	[MHz]	> 60 dB	> 60 dB
Over-voltage protection		See **Table 9**	See **Table 9**
Analog inputs 50 Ω mode (–PXIE and –MTCA)			
Input Impedance	[Ω]	50 ± 3 %	50 ± 3 %
Idle channel noise (Range 0.25)	[dBFS / Hz]	–135.8	–135.8
Idle channel noise (Range 0.5 1 2.5 5)	[dBFS / Hz]	–141.8	–141.8
Flatness –1 dB	[MHz]	200	200
Bandwidth upper limit –3 dB	[MHz]	500	500
Analog inputs 1 MΩ mode (–PXIE only)			
Input Impedance	[MΩ]	1 ± 3 %	–
Input capacitance	[pF]	15 ± 20 %	–
Bandwidth upper limit –3 dB	[MHz]	180	–
Analog input 50 Ω . Test signal at –1 dBFS at 72 MHz.			
SNR (Range 0.25 V_{pp})	[dBFS]	46.8	46.8
SNR (Range 0.5 1 2.5 5 V_{pp})	[dBFS]	52.8	52.8
SFDR (All ranges)	[dBFS]	57	57
ENOB (Range 0.25 V_{pp})	[bits]	7.5	7.5
ENOB (Range 0.5 1 2.5 5 V_{pp})	[bits]	8.1	8.1

1. The input impedance is software controlled individually per channel.
2. 1 MΩ is not available on –MTCA.
3. Rail-rail on all input range settings.
4. Rail-rail on all input range settings.

Table 2: Clock

PARAMETER		–PXIE	–MTCA
Internal Clock Reference			
Frequency	[MHz]	10 ± 3ppm	10 ± 3ppm
Drift		± 1 ppm / year	± 1 ppm / year
PXIe backplane clock reference			
PXIe sync	[MHz]	10	–
PXIe clock	[MHz]	100	–
MTCA.4 Backplane clock reference			
TCLK A	[MHz]	–	10
TCLK B	[MHz]	–	10
External clock reference			
Frequency	[MHz]	10	10
Clock reference output			
Frequency	[MHz]	10	10
External clock			
Clock frequency	[MHz]	1000	1000
Sample skip			
Ratio[1]		1 2 4 5 6 7... 2^{16}	1 2 4 5 6 7... 2^{16}
Front panel connector clock input			
Signal level minimum	[Vpp]	0.2	0.4
Signal level recommended	[Vpp]	0.6	1
Signal level Maximum	[Vpp]	0.8	2.8
Input impedance AC	[Ω]	50	50
Input impedance DC	[Ω]	10 k	10 k
Connector		SMA	SMA[2]
Front panel connector clock output			
Level (into 50 Ω, typical)	[V]	1.6	1.1
Output impedance AC	[Ω]	50	50
Output impedance DC	[Ω]	10 k	10 k
Coupling		AC	AC
Connector		MCX	SMA[2]

1. Sample skip ratio of 200 means that the data rate is reduced a factor of 200, that is from 1 GSPS to 5 MSPS.
2. Connector is shared between input and output. The direction is software controlled.

Table 3: Trigger

PARAMETER		–PXIE	–MTCA
Analog channel as trigger[1]			
Connector		LEMO00	SMA
Impedance DC	[Ω]	see **Table 1**	see **Table 1**
Signal level[2]	[V]	see **Table 1**	see **Table 1**
Signal swing	[Vpp]	see **Table 1**	see **Table 1**
Adjustable software controlled trigger threshold[3]	[V]	see **Table 1**	see **Table 1**
Time resolution (interpolated value)	[ps]	25	25
Jitter	[ps]	10	10
Star B backplane trigger			
Connector		Backplane	–
Time resolution	[ns]	4	–
MLVDS backplane trigger			
Connector		–	Backplane
Time resolution	[ns]	–	4
External trigger input on front panel			
Connector (shared with output)		SMA	SMA
Time resolution	[ns]	1	1
Adjustable threshold	[V]	0 to +3.0	0 to +3.0
Signal level	[V]	–0.5 to +3.3	–0.5 to +3.3
Input impedance	[Ω]	50	50
Input impedance high[4]	[Ω]	500	500
External trigger output on front panel			
Connector (shared with input)		SMA	SMA
Level (no load, typical)	[V]	0 to +3.3	0 to +3.3
Output impedance	[Ω]	50	50

1. Use one of the analog inputs as trigger. The timing of the trigger is interpolated to high accuracy.
2. Use the DC-offset and range settings to adjust to the trigger signal. See **Table 1** for details.
3. The setting of the threshold is within the signal range selected.
4. Software controlled high impedance for bussed connection.

Table 4: SYNC trigger signal

		–PXIE	–MTCA
Output			
Connector		MCX	SMA[1]
Impedance DC	[Ω]	50	50
Signal level output (no load)	[V]	0 to 3.3	0 to 3.3
Input			
Connector		MCX	SMA[1]
Impedance DC [2]	[Ω]	10 k	10 k
Threshold	[V]	1.6	1.6
Input synchronous mode[3]			
Time resolution	[ns]	100	100
Input asynchronous mode			
Time resolution	[ns]	4	4
Jitter asynchronous mode	[ns]	1.15	1.15

1. Connector is shared between input and output. The direction is software controlled.
2. The signal has to be source terminated to 50 Ω.
3. Synchronous mode phase locked to 10 MHz reference.

Table 5: General specifications

OPTION		–PXIE	–MTCA
Key parameters			
Channels		8	8
Sample rate / channel	[GSPS]	1	1
Resolution	[bits]	10	10
Data memory[1]	[GByte]	1	1
Data rate to host PC [2]	[GBPS]	2.6	1.6
Mechanical			
Weight	[g]	520	460
Board width including –VG	[slot]	2	Double width
Board height		3U	Mid size
Electrical			
Power supply	[V]	12	12
Power dissipation	[W]	46	46
Temperature range			
Operation	[°C]	0 to 45[3]	0 to 45
Storage	[°C]	–40 to 70	–40 to 70
Compliances			
CE		✓	✓
RoHS2		✓	✓
FCC		Exclusion according to CFR 47, part 15, paragraph 15.103(c)	

1. The data memory is shared between data from all channels.
2. Depends on the capacity of the chassis and controller PC.
3. High fan setting required if available on the chassis.

Table 6: Data acquisition parameters –FWDAQ: Multi-record

		STEP SIZE	MIN / MAX
Re-arm time	[us]	–	4
Pre-trigger length	[samples]	1	0 to record length
Trigger delay	[samples]	4	0 to 2^{32} –4
Record length	[samples]	1	50 M
Data transfer speed max	[GBytes/s]	–	3.2
Data transfer speed sustained	[GSamples/s]	–	1.3
Data memory	[samples per channel]	–	50 M

Table 7: Data acquisition parameters –FWDAQ: Streaming

		STEP SIZE	MIN / MAX
Re-arm time	[ns]	–	168
Pre-trigger length	[samples]	4	0 to 16 k
Trigger delay	[samples]	4	0 to 2^{32} –4
Record length	[samples]	4	4 to 50 M
Data transfer speed max	[GBytes/s]	–	3.2
Data transfer speed sustained	[GSamples/s]	–	1.3
Data memory	[samples per channel]	–	50 M

Table 8: Software support

	COMMENT
Operating systems[1]	
Windows 8 / 8.1, 32-bit and 64-bit	✓
Windows 10, 32-bit and 64-bit	✓
Linux	✓
Application	
GUI	Digitizer Studio[2]
C/C++	API, examples
Python	Example scripts

1. See “15-1494 Operating System Support” for supported distributions.
2. See 20-2381 Digitizer Studio Datasheet for supported hardware options, firmware options and operating systems.

2 Frequency response

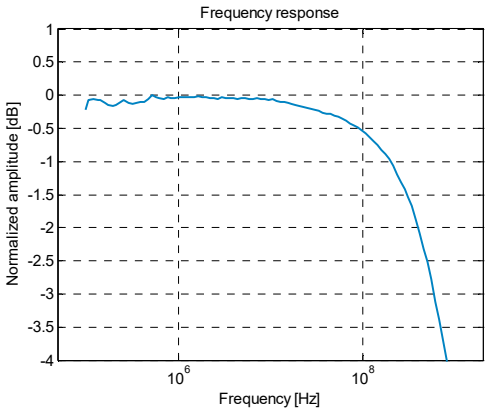


Figure 1: ADQ8-8C 50 Ω frequency response.

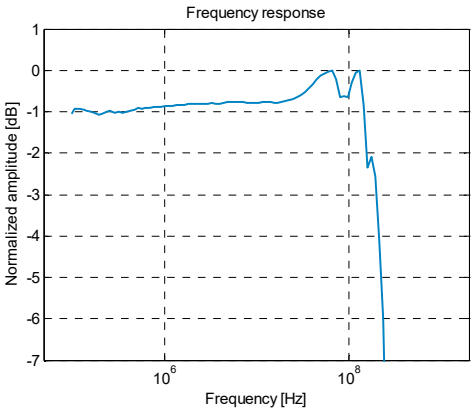


Figure 2: ADQ8-8C 1 MΩ frequency response.

3 Frequency domain

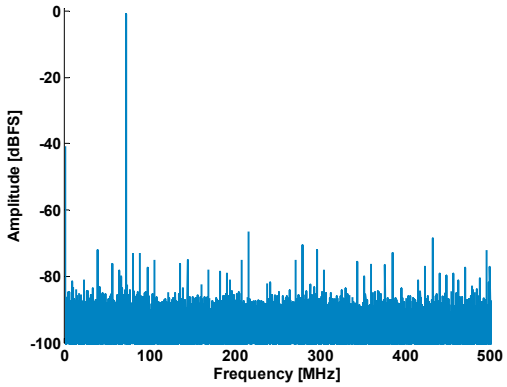


Figure 3: ADQ8-8C 50 Ω frequency domain plot.

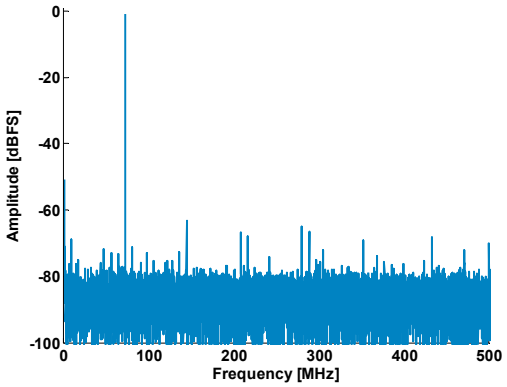


Figure 4: ADQ8-8C 1 MΩ frequency domain plot.

4 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device. The analog inputs are protected from over-voltage but the values in **Table 9** must never be exceeded.

The built-in temperature monitoring unit will protect the ADQ8-8C from overheating by temporarily shutting down parts of the device in an overheat situation.

The PXIe

Table 9: Absolute Maximum Ratings

PARAMETER		MIN	MAX
Analog input 50 Ohm[1]			
Voltage to GND	[V]	– 5.0	+ 5.0
Analog input 1 MOhm			
Voltage to GND	[V]	– 5.0	+ 5.0
Trigger			
Voltage to GND	[V]	–2.3	5.0
SYNC			
Voltage to GND	[V]	–0.3	+3.6
CLKIN			
Voltage to GND	[V]	–5	+5
Power supply			
Voltage to GND	[V]	–0.4	14
Temperature			
Operating (min, max)	[°C]	0	45

1. Also valid for analog channel used as trigger.

5 Block diagram

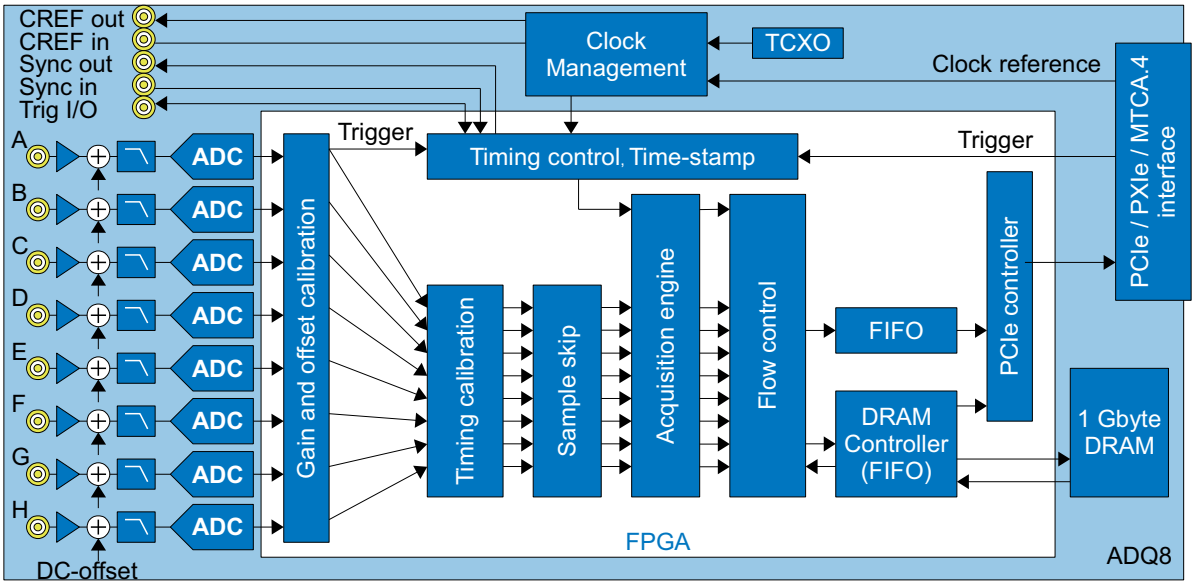


Figure 5: Block diagram for ADQ8-8C

6 Integrating the ADQ8-8C

ADQ8-8C is a multi-channel digitizer for modular instrumentation. **Figure 6** illustrates how ADQ8-8C supports the key parts of the system integration.

6.1 Detecting the analog signal

The analog front-end is optimized for high density system. The DC-coupled front-end has high sensitivity to simplify the interfacing to the detector. DC-offset effectively doubles resolution for uni-polar pulses.

To handle a variety of detectors, there is an advance analog front-end option with impedance control, 50 Ω or 1 MΩ [1] and voltage range settings.

6.2 Timing and synchronization

The clock management and trigger support connects with the infrastructure of the system.

Clock reference is either internal for stand-alone operation or from the chassis for synchronized system. The trigger signal and synchronization network align acquisition in multiple units. The time-stamp allows for accurate post-processing of data from channels on different digitizers. The trigger timing interpolation increase the trigger resolution.

6.3 Real-time processing

The data acquisition engine in the FPGA supports acquisition of real-time events. Set up pre-trigger and trigger delay to capture the at the correct moment relative to the trigger to minimize the data set and thereby the load on the host PC.

1. 1 MΩ is not available on –MTCA.

6.4 System integration

The ADQ8-8C is optimized for robust large scale integration in a PXIe or MTCA.4 chassis. The electrical properties, shielding and power supply in these chassis allows for high channel count.

6.5 Software tools for building the application

The software development kit is a software package that contains the ADQAPI, drivers and example code for integrating the ADQ8-8C into the application. The ADQAPI is the programmers interface for the ADQ8-8C. It contains low level functions for efficient solutions as well as high level support for quick and easy access to the function.

The many examples and application notes simplify the integration process and shorten the time-to-market.

The SDK is included free of charge with the ADQ8-8C.

6.6 Digitizer Studio GUI

The ADQ8-8C is supplied with the Digitizer Studio software providing quick and easy control of the digitizer. The tool offers both time-domain and frequency-domain analysis. Data can be saved in different file formats for off-line analysis. With Digitizer Studio, the ADQ8-8C operates as a stand-alone measurement instrument.

Note that Digitizer Studio only implements a subset of the flexibility of the ADQ8-8C. The full potential of the ADQ8-8C is reached using the SDK. For more information on Digitizer Studio see 20-2381 Datasheet and 20-2382 User Guide.

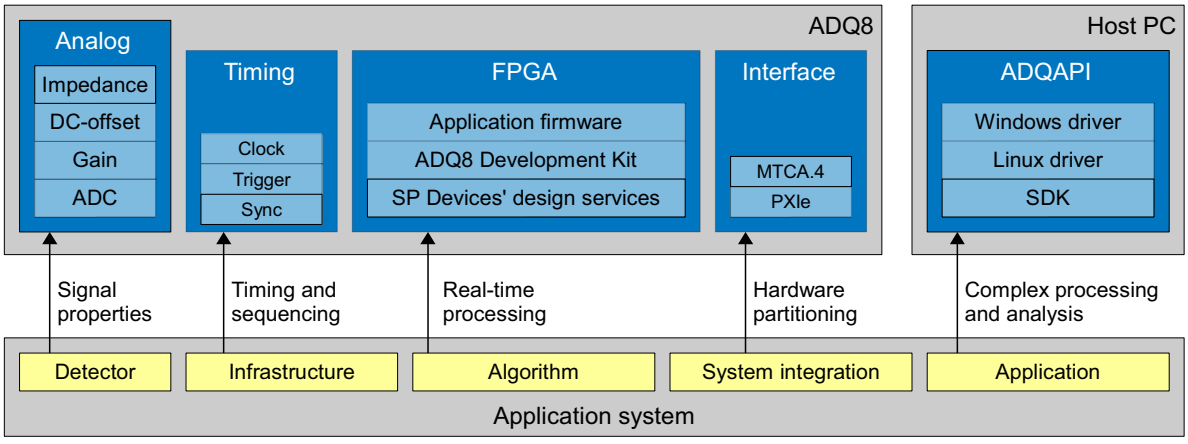
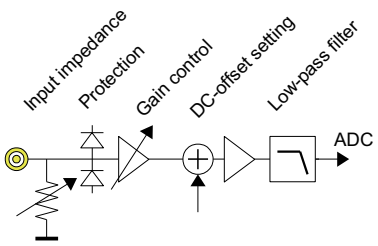


Figure 6: Integrating the ADQ8-8C into the system.

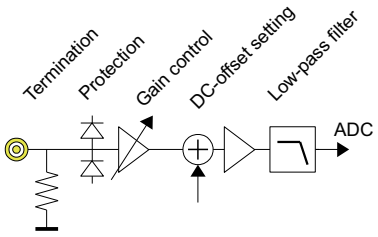
7 Analog front-end



Analog front-end ADQ8-8C–VG–PXIE

The full flexible analog front-end offers input impedance settings 50 ΩOhms or 1 MΩ, DC-offset and signal range control through software commands.

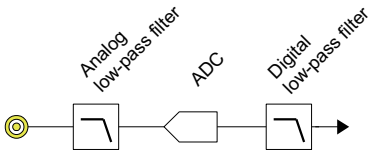
The over-voltage protection, low pass anti-aliasing filter of are also available.



Analog front-end ADQ8-8C–VG–MTCA

The full flexible analog front-end has a fixed input impedance of 50 Ω. DC-offset and signal range control is available through software commands.

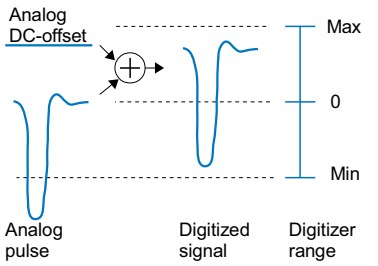
The over-voltage protection, low pass anti-aliasing filter of are also available.



Bandwidth control

The analog input is DC-coupled with an analog bandwidth of 500 MHz. The analog low pass function is acting as an anti-aliasing filter.

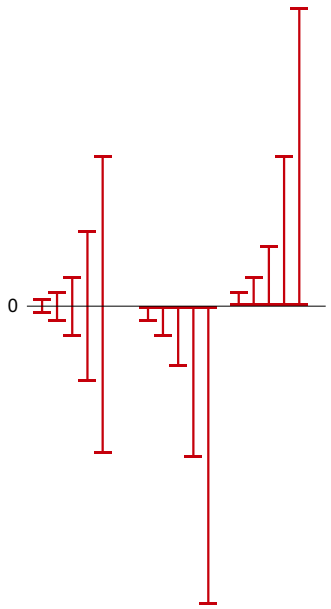
The signal bandwidth can then limited by a user controlled digital filter. This filter improves the SNR for band-limited signals.



DC-offset

The DC-offset is an analog DC-level added to the analog signal for acquisition of uni-polar pulses. The DC-offset effectively doubles the resolution for this type of signals. The DC-offset level is controlled rail-to-rail from a software command.

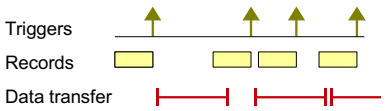
The DC-offset can handle positive and negative pulses.



Gain control –VG (input range setting)

The variable gain function –VG enable control of the analog signal range. Combine the range setting with the DC-offset for full control of the analog signal properties.

8 Data recording

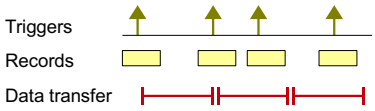


Multi-record

At each trigger, a record (set of continuous data) is captured. The record is buffered in the a circular buffer in the DRAM. Using the DRAM as a circular buffer enables the use of a very long pre-trigger. The pre-trigger can be set to the length of the record.

The number of records is either a fixed amount after which the acquisition is stopped or an unlimited acquisition which continue until the user stops it.

Operate ADQ8-8C in a single record mode by setting the number of records to one.



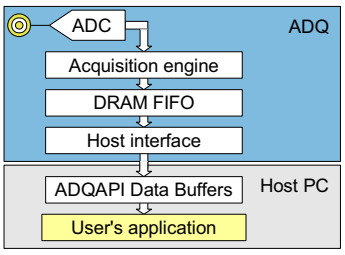
Streaming

At each trigger, a record (set of continuous data) is captured in the DRAM acting as a FIFO ready to be streamed to the PC. This mode is for high throughput continuous operation.

The number of records is either a fixed amount after which the acquisition is stopped or an unlimited acquisition which continue until the user stops it.

Operate ADQ8-8C in a single record mode by setting the number of records to one.

Streaming is described in 20-2465.

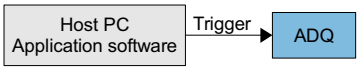


Data Transfer

Large FIFO Guarantees reliable data transfer.

There is 1 GBytes of on-board DRAM which is typically used as a large FIFO. The FIFO guarantees stable operation over a long time at high data rates. The large FIFO also enables bursts of triggers at high rate. The Gen2 x8 PXIe interface enables high speed data transfer.

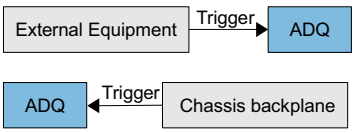
9 Trigger module



Software trigger

This is a user-controlled trigger.

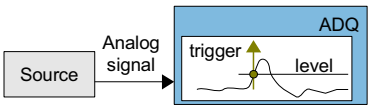
The software trigger is activated from the user's application software. It is used for building oscilloscope applications. The software trigger can also be used for a watch-dog application for surveillance of the experiment.



External trigger

This is for synchronizing the acquisition to an experiment.

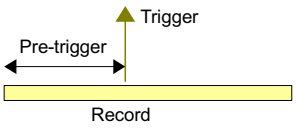
The external trigger is a signal from another unit that initiates the acquisition. External trigger inputs are available on the front panel by using channel A and in the PXIe backplane (star trigger).



Level trigger

This is a data driven acquisition.

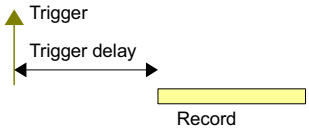
The level trigger reacts when the analog input goes above or below a programmable level.



Pre-trigger buffer

Capture data before the trigger.

The pre-trigger buffer allows for capturing of data long before the trigger event occurred. This is useful for analyzing the cause of an event.

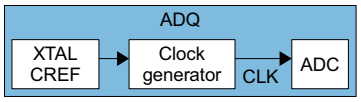


Trigger delay

Capture data long after the trigger event.

The trigger delay feature inserts a delay from the trigger event until data collection starts. It is used to reduce the amount of captured data when the interesting signal is known to occur a certain amount of time after the trigger event.

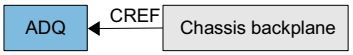
10 Clock module



Internal clock

High precision clock for stand-alone operation.

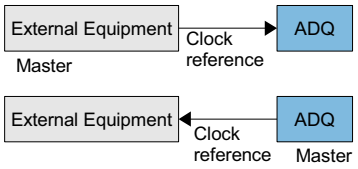
The ADQ8-8C is clocked by an internal clock source. The clock reference is an internal high quality temperature compensated crystal oscillator.



Clock reference from back plane

This is for synchronizing multiple ADQ8-8C.

The internal clock generator is locked to an externally provided frequency reference. The frequency reference is provided via the PXIe backplane.

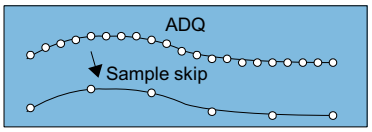


External clock reference

This is for synchronizing the acquisition to an experiment.

The internal clock generator can be used as cock reference to an external device.

The ADQ8-8C can also be synchronized to an external device through the clock reference input.

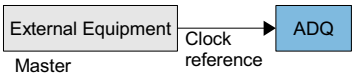


Sample skip

For adapting the sample rate to the situation and optimize the amount of data.

The sample skip function can easily adjust the sample rate to limit the amount of data. The ADQ8-8C can then adapt to changing situations.

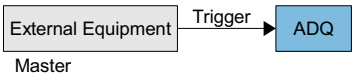
11 Synchronization support



Clock reference input

Sharing clock reference guarantees a common time base.

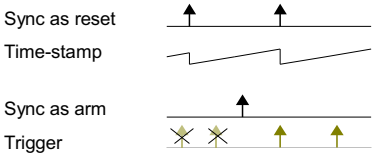
Use the clock reference input when the external equipment supply the clock reference. The clock reference from the chassis back-plane can be used to synchronize several ADQ8-8C.



Trigger input

The trigger starts the operation simultaneously.

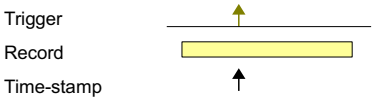
The trigger marks the start of an operation. The ADQ8-8C can take a trigger as input to start the acquisition.



Synchronization input and output

Extra trigger to mark beginning of a sequence.

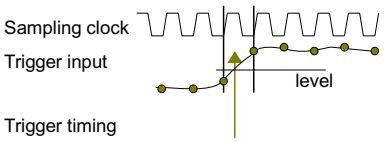
The sync pin can be used as an input for resetting the time-stamp counter. It can also be used as an output for broadcasting a trigger to several ADQ8-8C units.



Time-stamp

A real-time value for each trigger.

The time-stamp is a real-time value for each trigger event. The time-stamp allows precise analysis of the timing relationship of different acquisitions from the same or different ADQ8-8C units.

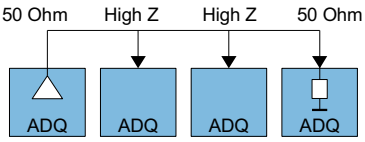


Sub-sample precision time-stamp

High precision external trigger.

The external trigger timing precision is 25 ps which enables precise timing analysis. This is enabled by using Channel A as a Trigger input.

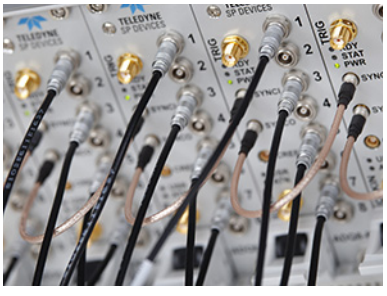
The subsample precision of the trigger also enables accurate synchronization of a large system.



Bussed connection

Save cabling by bussed connections.

The sync signal can be set in high impedance mode to enable bussed connections.For best signal integrity minimize the length of the unterminated stubs.

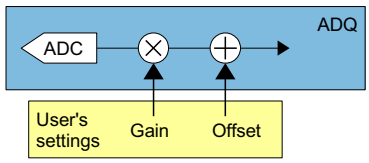


Large scale synchronization

Simultaneous triggering of a full chassis.

The sync signal can be daisy chained to all boards in a chassis. The trigger in can then be distributed to all boards in a chassis. Factory calibration is offered to get a trigger precision better than 200ps.

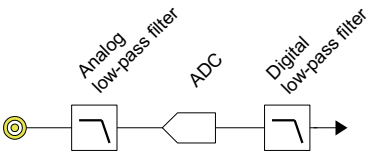
12 Built-in signal processing



Gain and offset calibration

Digital signal tuning in the FPGA.

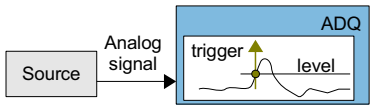
The user can set gain and offset parameters that are applied to the digitized signal immediately after the analog-to-digital converters. This can e.g. be useful to compensate for system offsets and simplify later signal processing in the host computer.



Digital filter

Bandwidth control and noise reduction.

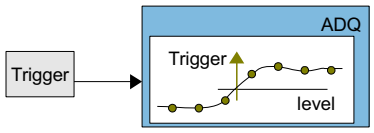
The analog bandwidth is set allow to 500 MHz. To get a precise frequency response there is a digital filter to set the bandwidth and the frequency response.



Level trigger

Data driven acquisition.

The level trigger enables data driven acquisition.



Trigger timing

Accurate trigger timing.

Use channel A as a high accuracy trigger. The trigger timing is calculated to 25 ps resolution. In a multichannel system, there is support for multi-unit calibration and triggering.

13 Form factor and data interface

Modular instrumentation with cPCIe / PXIe (–PXIE)

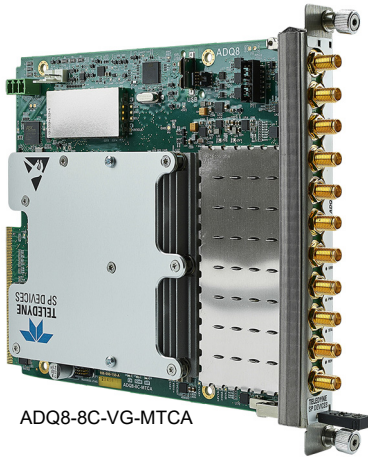
ADQ8-8C-VG-PXIe

- Modular instrumentation

The cPCIe / PXIe form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition. The ADQ8-8C can operate in Compact PCI Express or PXI Express chassis. Using the multi-unit sync function, multi-channels systems can be achieved.

In a PXI Express chassis, the clock reference from the backplane can be used as clock reference for the digitizer. Backplane trigger (Star B) is also supported to simplify integration.

Modular instrumentation with MTCA.4 (–MTCA)



ADQ8-8C-VG-MTCA

- Modular instrumentation

The MTCA.4 form factor is intended for integration into a chassis for modular instrumentation or large scale acquisition.

PXIExpress™ µTCA® KINTEX 7 WARRANTY THREE 3 YEAR WARRANTY

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Teledyne SP Devices Corporate Headquarters

Teknikringen 6
SE-583 30 Linköping
Sweden

Phone: +46 (0)13 465 0600
Fax: +46 (0)13 991 3044
Email: info@spdevices.com